Implementation of a Scalable and Statistical VBIC Model for Large-Signal and Intermodulation Distortion Analysis of SiGe HBTs

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Abstract - **This work examines for the first time the utility of the VBIC model for the analysis of 2-tone intermodulation distortion behavior of SiGe HBTs. The model takes into account all important effects for accurate modeling of large signal behavior including self-heating, weak-avalanche multiplication, quasi-saturation effects, and all device capacitances. Periodic-Steady State and Harmonic Balance simulations are performed and the model is validated by load-pull measurements.**

I. INTRODUCTION

With the emergence of Silicon-Germanium HBTs as a powerful contender for RF power amplifiers in wireless applications, there is an urgent requirement to develop transistor compact models that can be used for accurate simulation of circuit large-signal behavior using commercial CAD tools, and which can be directly incorporated into BiCMOS design kits. It is equally important to examine how standard bipolar compact models themselves perform under large signal conditions and how to improve them to accurately model the output power, harmonics and intermodulation distortion characteristics. While the SPICE Gummel-Poon model is known to be inadequate to describe many of the physical effects important for high-speed Bipolar transistors [1], very little effort has been made to exploit more advanced bipoar models such as VBIC, HiCUM or MEXTRAM for modeling distortion [2, 3].

Methods employing the Volterra series approach for distortion analysis provide good insight for the determination of dominant non-linearities in the device, but their utility is limited largely to the regime of weak non-linearities. On the other hand, it is of significant practical interest to accurately model well into the compression regime where most analytical approximation methods fail. Classical time-domain transient analysis with a 2-tone excitation followed by a Fourier analysis can in principle compute large-signal distortion, but it is quite inefficient since the RF frequency is several orders of magnitude larger than the baseband frequencies, thus requiring an enormous number of time steps. This leaves Harmonic Balance (HB) [4] and Shooting Methods, such as Periodic Steady State (PSS) [5] as the suitable methods for simulating large-signal behavior of circuits.

In this paper, the VBIC model is employed to study intermodulation distortion characteristics of a state-of-the-art high voltage SiGe HBT. In section II, the device cross-section and the technology are briefly described. Load-pull measurements used for the validation of the model are described in section III. The extraction of the VBIC model for the high-voltage SiGe HBT is described in section IV. Large-signal analyses comparing HB and PSS simulations are described in section V. Results of model vs. measurement for the output power at fundamental and 3rd and 5th order intermodulation frequencies for a 0.44 μm x 47.7 μm and 0.44 μm x 12 μm x 2 SiGe HBT are described in section VI.

II. TECHNOLOGY

HBTs were fabricated using IBM's 0.24μm UHV/CVD commercial SiGe BiCMOS technology targeted for mixed-signal RF applications (Fig. 1) [6]. The fabrication is performed with the base-after-gate approach, enabling SiGe base process to be decoupled from the high thermal budget of the CMOS devices. Substrate isolation and reduction of noise coupling is achieved through both shallow and polysilicon-filled deep trench isolation surrounding all HBT devices. Additionally, a thick

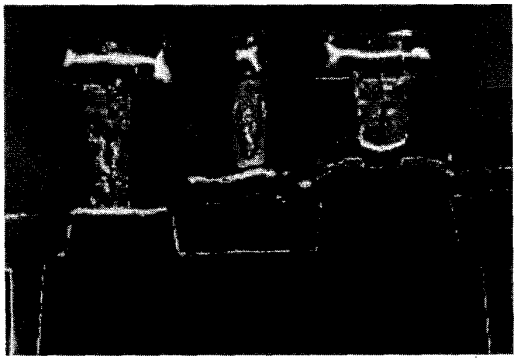

Fig. 1. SEM cross section of a self-aligned SiGe HBT with shallow and deep trench isolation.

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dielectric/metal add-on module [6] is included for high performance passive components needed for RF applications.

Self-aligned HBT devices in this technology includes both a high performance (HP) SiGe HBT with an f_T = 47 GHz and a BVCEO=3.3V for low-noise applications, and a high breakdown (HB) device with a f_T = 27GHz and a BVCEO=5.5V for high power output stages. Both HBTs are similar except for the tailored selectively implanted collector (SIC) profile. Careful optimization of the SIC implant is not only important both for suppression of Kirk efftect and BVCEO tradeoff, but also for minimization of the M-1 avalanche multiplication nonlinearity that can degrade the intermodulation performance [7].

III. MEASUREMENTS

Current-voltage (I-V) and capacitance-voltage (C-V) measurements were performed on devices with Kelvin padsets, while the RF measurements were performed on a G-S-G padset arrangement with the substrate connection routed underneath the ground pad. A 2-tier technique employing on-wafer open and short test structures was used for de-embedding pad and wiring parasitics. Load pull 2-tone measurements are performed using an ATN system that employs electronic tuners. The two input tones were 900 MHz and 900.1 MHz. The output matching was configured for maximum output power with the input conjugately matched. This is done at the 1 dB compression point. Better output power levels and PAE were observed with forced Vbe rather than forced Ib, as was also reported previously [8].

IV. MODEL DEVELOPMENT

Specific test structures were used for the determination of the external and internal base resistance, collector, and subcollector resistances. Base resistance was also extracted from the S11 data using the standard input impedance circle method. Large area capacitance monitor structures were specially designed and used to extract the area and perimeter components of each relevant junction capacitance, emitter overlap capacitance, extrinsic base-collector capacitances etc. The capacitances are modeled by the classical C-V equation containing C_0, Vbi and m.

The drawn emitter dimensions are corrected for process-induced changes, such as corner rounding and length foreshortening of the emitter. Such a correction proved to be critical for determining correct scaling behavior [9]. The area and perimeter components of the saturation currents, both for forward Gummel and reverse Gummel are determined by analyzing structures with varying emitter dimensions. High current behavior is modeled taking into account the resistive as well as high-injection effects.

Modeling the quasi-saturation behavior correctly was found to be essential for the large-signal and intermodulation distortion characteristics. Quasi-saturation effects, which result from the base-collector junction being forward biased, are more pronounced for the high breakdown device family since these devices have a lightly doped collector region, resulting in higher intrinsic collector resistance.

Self-heating of the device was modeled in VBIC using a thermal resistance and capacitance sub-circuit. Breakdown due to weak-avalanche multiplication is modeled using the models derived by Kloosterman, et al., [10] with the impact ionization parameters fit to experimental output curves. The scaling equations, process statistical variations and the model parameters are coded into a model file and optimizations are performed using the built-in VBIC equations in Spectre (Cadence Design System™) to obtain the VBIC parameters.

V. LARGE SIGNAL SIMULATIONS

First it is ascertained that the DC, S-parameters (up to 50 GHz) and f_T-Ic curves (as a function of Vcb) are modeled accurately before attempting to perform large-signal and distortion analysis. 2-tone simulations are then performed using PSS and HB to obtain power at the fundamental and intermodulation frequencies ($2f_1$-f_2, $2f_2$-f_1 and $3f_1$-$2f_2$, $3f_2$-$2f_1$). The modeled device was biased through a 1 µH RF choke (L) and a 1 µF blocking capacitor (C). For values smaller than these, the simulator produced inaccurate results such as dependence of Pout on L and C at certain biasing conditions etc. Matching conditions at the input and output are obtained from the load-pull measurement and the network is implemented with ideal elements.

In Spectre (Cadence Design System™) PSS the tolerances ('reltol') had to be relaxed to 1e-3 to achieve convergence at higher input power levels, especially in the compression regime. In the HB simulations (Advanced Design System, Agilent Technolgies™) the 'order' was found to be very important, for example, inaccurate results were obtained for IM3 and IM5 if the order is less than 7, though the simulation time is long for an order of 7. Accurate results were obtained in HB by implementing the input and output matching networks with lumped elements rather than using a complex Z port termination.

VI. RESULTS

Fig 2 shows the measured Ic-Vce characteristics compared with VBIC model simulations for a 0.44 µm x 47.7 µm device. Reasonable agreement can be seen in all

the four regions -saturation, quasi-saturation, linear region and the breakdown region.

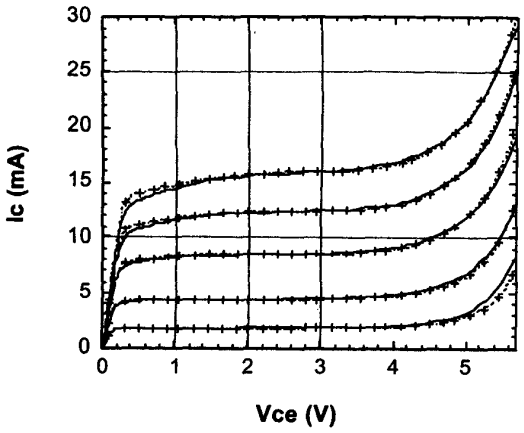

Fig. 2. The output curves of a 0.44 μm x 47.7 μm SiGe HBT for Ib = 24, 60, 120, 180 and 240 μA.

—— measured, •••+••• VBIC model

Figure 3 shows measurement and model comparisons of Pout, IM3 and IM5 for a 0.44 μm x 47.7 μm device for a collector current of 17 mA (nearly peak f_T) at a Vce of 3.3V. It can be seen that the models track Pout and IM3 reasonably well even in the compression regime while IM5 shows some discrepancies.

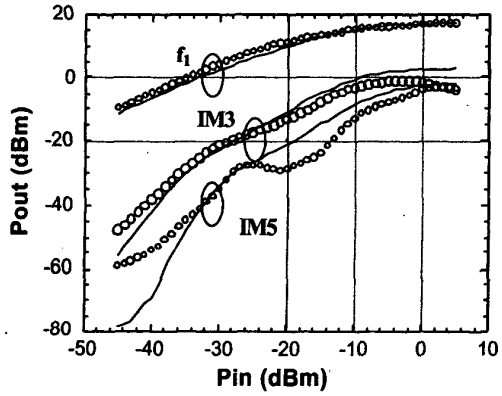

Fig. 3. Variation of Pout at the fundamental and 3rd order and 5th order intermodulation frequencies for a 0.44 μm x 47.7 μm SiGe HBT. - = Measurement, O = HB simulations

The scalability of the models was checked for device sizes ranging from 0.32 μm x 1.04 μm to 0.44 μm x 47.7 μm (including some dual finger devices) and for DC, S parameter and temperature dependence characteristics. Fig 4 shows the characteristics for a 0.44 μm x 12 μm x 2 device, where we also show comparisons between PSS and HB. PSS simulations could not be carried out far into compression due to convergence problems. Better correlations could be expected if the 'order' is increased to a higher number in the HB simulations, though it amounts to larger simulation times.

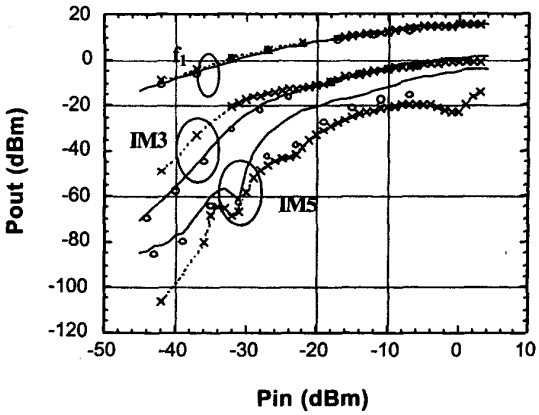

Fig. 4. Variation of Pout at the fundamental and 3rd order and 5th order intermodulation frequencies for a 0.44 μm x 12 μm x 2 SiGe HBT.
— = Measurement, ···X··· = HB simulations and O = PSS simulations using the VBIC model

VII. CONCLUSIONS

A scalable VBIC model has been developed for high voltage SiGe HBTs and the linearity performance is validated with load-pull measurements. Satisfactory agreement is seen for fundamental and IM3 performance well into compression. The accuracy of the IMD results were found to be dependent to some extent on the simulation method used (PSS or HB)

REFERENCES

1. C.C.McAndrew et.al, "VBIC95, the vertical Bipolar inter-company model", *IEEE. J. Solid State Circuits*, Vol. 31, 1996
2. M. Schroter, D. R. Pehlke, T-Y. Lee, "Compact Modeling of High Frequency Distortion in Silicon Integrated Bipolar

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Transistors", IEEE Trans. On Electron Devices, Vol.47, pp 1529-35, 7 July 2000
3. L.C.N. de Vreede et.al, " Advanced modelling of Distortion effects in Bipolar Transistors using the Mextram Model", *Proc.of IEEE BiCMOS Circuits & Technology Meeting*, page 48, 1994.
4. Cadence SpectreRF 4.4.6 User's Guide
5. Agilent's ADS 2001 User's Guide
6. S.A. St. Onge et.al, "A 0.24um SiGe BiCMOS mixed-signal RF production technology featuring a 47 GHz ft HBT and 0.18mm Leff CMOS," *Proc. IEEE BiCMOS Circuits & Technology Meeting*, pp. 117-120, Sept. 1999.
7. G. Niu, Q. Liang, J.D. Cressler, C.S. Webster, D.L. Harame, "RF linearity characteristics of SiGe HBTs," *IEEE Trans. Microwave Theory and Tech.*, vol. MTT-49, no. 9, pp. 1558-1565, Sept. 2001.
8. D. A. Teeter et.al., "Use of Self Bias to Improve Power Saturation and Intermodulation Distortion in CW Class B HBT Operation", *IEEE Microwave and Guided Wave Letters*, Vol.2, pp 174-76, May 1995
9. K.Walter et. al, *Proc. IEEE BiCMOS Circuits & Technology Meeting*, pp.32-35, 1997.
10. W.J. Kloosterman, J.C.J. Paaschens, R.J. Havens, "A comprehensive bipolar avalanche multiplication compact model for circuit simulaiton," *Proc. IEEE BiCMOS Circuits & Technology Meeting*, pp. 172-175, 2000.